# A complete Narrow-Band Power Line Communication node for AMR


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***Abstract-*** **In this paper it is reported the description of a demonstrator implementing a low data rate Power Line Communication node, developed for Automated Meter Reading applications. This study is focused on investigating those aspects of the communication node design impacting most on the requirements for compliance with communication on the electrical network environment. Design choices, compliance tests, thermal analysis and experimental results are described in this paper.**



***Index Terms-*** **Power line communication, automated meter reading, analog front-end, power amplifier, line coupling, thermal impedance.**


## I. Introduction

When designing a Power Line Communication (PLC) node, attention is required to make this node capable to operate in a complex and challenging environment like the power line. One of the most restrictive requirements is the compliance with the European EN50065 standard for signaling on low voltage electrical networks [1].

The requirements set by this standard are not only related to conducted emissions, according to EN50065-1, but also to impedance magnitude limits fixed by EN50065-7 and to immunity against conducted interferences as required by EN50065-2-1.

The specific structure of the coupling interface is a weak point of the application against high voltage disturbances that can come from the external environment. The immunity requirements to be addressed are the ones listed in the EN50065-2-1 document, which refers to EN61000-4 for the tests to be applied [2].

Analysis of the thermal behavior with respect to the required output power is fundamental for a PLC node design. Such analysis has to take into account the operating conditions of a typical Automated Meter Reading (AMR) application, which is the target application for the described PLC solution. A thermal study, oriented to EN50065-1 compliance, is presented in this paper.

## II. Description of the Communication Node Demonstrator

The PLC communication node described in this paper has been designed to operate within the so called A-band, from 9 to 95 kHz, dedicated to AMR. The architecture of the PLC node demonstrator is reported in the block diagram of Fig. 1, which shows the various sections of the module. The demonstrator hosts the new ST7540 FSK power line transceiver, supplied by a Switching Mode Power Supply (SMPS) in flyback configuration, and controlled by an external host. The external circuitry for the PLC transceiver is composed of a 16 MHz crystal resonator driven by the internal oscillator, a passive R-C network for the transmission active filter based on the internal

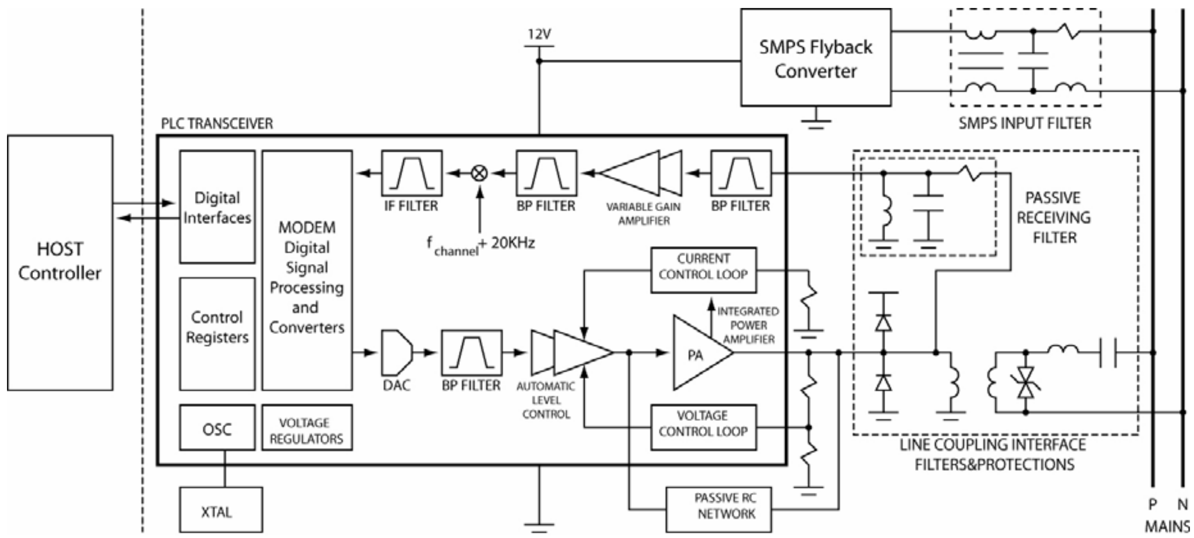


Fig. 1. Block diagram of the PLC node demonstrator

Power Amplifier (PA), and the line coupling interface including passive filters and protections against high energy disturbances from the line.

A photograph of the PLC demonstrator is shown in Fig. 2. The three main sections are highlighted: the SMPS section, the transceiver IC section and the line coupling interface.

Description of the transmission active filter, the coupling interface and the SMPS is included below.

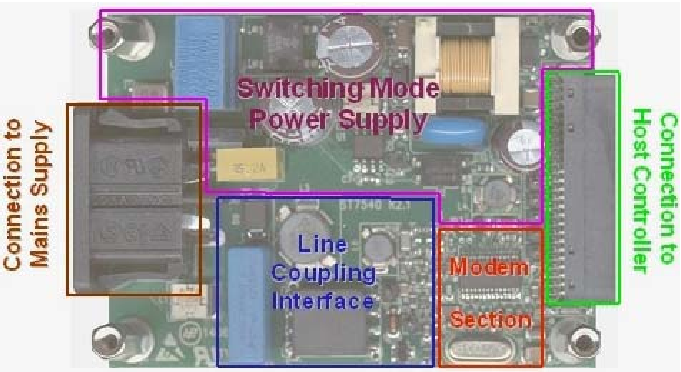


Fig. 2. Photograph of the PLC node demonstrator with its different sections

## A. *Transmission Active Filter*

The integrated PA of the transceiver, whose input and output lines are externally available, has been configured to implement an active filter whose schematic is reported in Fig. 3. It is a 3-pole active filter, made up of the R3-C2 low-pass stage and of a 2-pole Sallen-Key cell. Capacitor C1 for dc decoupling and R1-R2 resistor partitioning are included to set the optimum bias for the PA input.

A Chebyshev type low-pass filter has been chosen to have high rejection on 2$^{nd}$ harmonic of the transmitted signal, well higher than the rejection obtainable with a passive filtering.

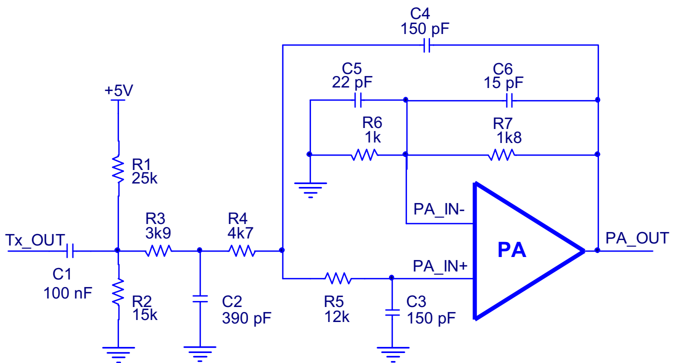


Fig. 3. Schematic of the active Tx filter based on the integrated PA

The filter has been dimensioned to have a dc gain of 9 dB, to get the correct output bias (depending on the input bias multiplied by the dc gain) and to exploit the output voltage dynamic range. Both factors contribute to obtain high linearity. Measured frequency response is shown in Fig. 4. The filter, designed for the 72 kHz channel, has a corner frequency at 87 kHz, a maximum ripple of 1 dB and a 2$^{nd}$ harmonic rejection of about 9 dB at 144 kHz.

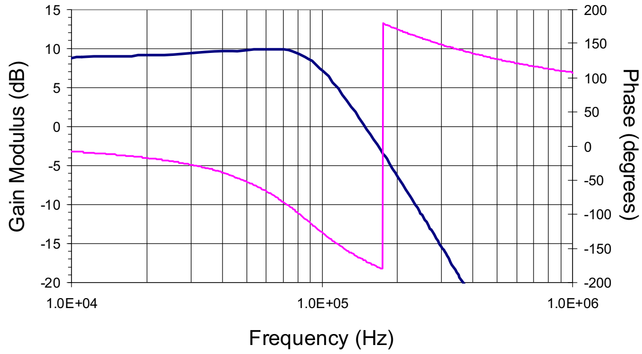


Fig. 4. Typical frequency response of the active filter

## B. *Line Coupling Interface*

Interfacing to the power line requires a passive circuit to obtain selective coupling for the signal in transmission and reception. This requires both an adequate frequency response, to ensure good performance on the communication channel, and correct impedance at the line connection, to comply with EN50065-7 requirements on the impedance seen from the line.

It has been chosen the coupling topology shown in Fig. 5. The 50 Hz mains voltage is filtered by the L-C high-pass filter made up of C8, L1 and the magnetizing inductance of the transformer T1 (about 1 mH). The transmitted signal coupling includes capacitor C7 for dc decoupling, L1-C8 series resonance for band-pass filtering and transformer T1 for high voltage isolation. The receiving filter is made up of series resistor R8, L2-C9 parallel resonant circuit for band-pass response and capacitor C10 for dc decoupling at the receiver's input.

This line coupling topology includes a protection structure capable to clamp high energy disturbances coming from the mains as either differential or common mode interferences. The protection structure is made up of D1 and D2, aimed at clamping fast common mode disturbances, and D3, for absorbing high energy differential disturbances. T1 also introduces suppression of common mode disturbances.

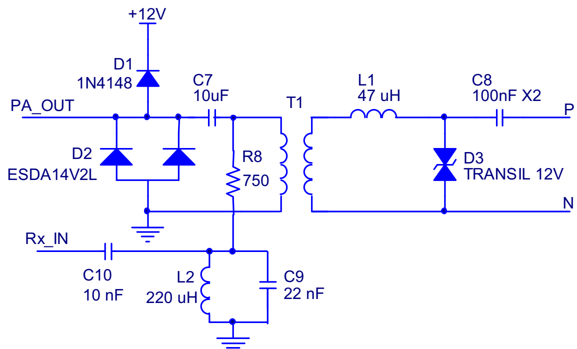


Fig. 5. Schematic of the line coupling circuit

## C. *Switching Mode Power Supply*

The small size and good efficiency (η = 70% at full load) power supply included in the PLC node demonstrator has been designed for compatibility with the PLC communication. A SMPS is required to supply a power amplifier having 35%

efficiency and driving the power line, which typically shows very low impedance. The SMPS output voltage of 12 V dc sets the dynamic range of the PA output signal to 7.5 V peak-to-peak, within which the PA output stage will show a linear behavior.

The input filter of Fig. 6 has been introduced at the mains connection of the SMPS. One purpose of the filter is to reject disturbances generated at switching frequency by the power supply. Common mode conducted emissions are filtered by common mode choke L4, while differential mode conducted emissions are reduced by the leakage inductance of L4 and the X2 safety capacitor C11.

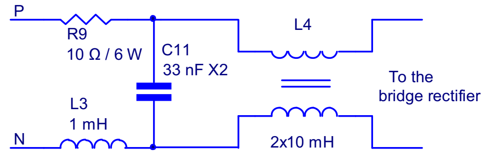


Fig. 6. Schematic of the input filter for the SMPS

This specific input filter implementation is also aimed at ensuring that the SMPS shows input impedance being as high as possible at the communication frequency, for compatibility with the PLC transceiver. In particular, inductor L3 and resistor R9 prevent the transceiver from being loaded by the low impedance of C11.

R9 is also designed in order to damp the resonant circuit composed of L3, C11 and the transceiver's line coupling circuit. R9 value is chosen as a compromise between SMPS efficiency and robustness against high voltage disturbances from the line.

## III. PLC Transceiver Architecture

The module is built around the new ST7540 FSK transceiver, realized in Multipower BCD 0.6 µm technology to allow the integration of digital, analog and power circuitry in the same chip [3]. It operates from a single 12V power supply.

The internal block diagram of the IC is shown in Fig. 1. The SPI host interface allows setting the operating parameters of the device through access to the internal Control Register. Eight different communication channels are available; six of them (60, 66, 72, 76, 82.05, 86 kHz) are within the A-band. For our tests, the IC has been programmed to communicate at 72 kHz channel frequency, 4800 baud and deviation 1, as the parameters for the binary FSK modulation.

### A. Analog Front-End and Power Amplifier

The transmitted signal is generated by a Digital Direct Synthesis (DDS) circuit at channel frequency plus or minus the frequency deviation set by the programmed baud rate. The digital signal is converted to analog by an 8-bit DAC and properly filtered. The filtered signal is then regulated by an Automatic Level Control (ALC) block, driven by the voltage and current automated controls. The IC integrates a class AB linear Power Amplifier able to provide an output signal for the ST7540 transceiver up to 130 dBµV rms. The behaviour of the ALC block is illustrated by Fig. 7. An external resistor partitioning fixes the desired PA output voltage level, kept constant by the ALC until the load impedance goes under a $Z_{LIMIT}$ value corresponding to the current limit, set by another external resistor. If the current limit is reached, the PA output voltage level is reduced step by step until the output current is again under the threshold value.

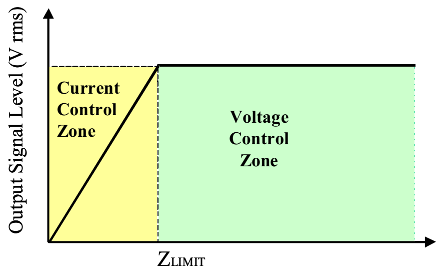


Fig. 7. Output voltage level vs. line load

## IV. Normative Requirements and Tests

### A. Spectrum of the Transmitted Signal

The EN50065-1 document sets the limits for transmission level and spurious conducted disturbances of equipments communicating within the A-band. Those limits refer to the signal measured on the 50Ω measure port of the artificial mains network defined by CISPR 16-1 document [4]. Different limits on the transmission level are set for narrow-band and wide-band signals. If the signal bandwidth at -20 dB is equal to or greater than 5 kHz, the signal is considered as wide-band and the limit is defined as 134 dBµV rms over the whole signal bandwidth and 120 dBµV rms when measuring with a peak detector having a bandwidth of 200 Hz. In the case of an FSK modulation, the main constraint is the spectral density limited at 120 dBµV rms, because the FSK spectrum is characterized by two narrow peaks corresponding to "0" and "1" symbols.

### B. Immunity Requirements

The most disturbing interferences for a PLC node are surges and fast transients from the line. For this kind of disturbances, the EN50065-2-1 document requires to perform the immunity tests described in Table I. The criterion for compliance is that a temporary degradation or loss of function, with automatic recovery, may occur, while no change in operating state is allowed.

TABLE I
Immunity Tests

| Test Type | Test Specifications | Basic Standard |
|---|---|---|
| Surges | Trise =1.2 us, Thold =50 us<br>1 kV common mode (peak)<br>0.5 kV differential (peak) | EN61000-4-5 |
| Fast transients | Trise =5 us, Thold =50 ns<br>1 kV (peak)<br>5 kHz frequency | EN61000-4-4 |

### C. Input Impedance

EN50065-7 document sets the impedance constraints for equipment operating in the A-band. The purpose is to avoid introducing attenuation on signals from other devices on the line. Impedance limit masks are shown in Fig. 10 and Fig. 11.

### D. Compliance Measurements

First of all, the compliance with the limits on the output spectrum has been verified. For this purpose, wide-band case has been addressed, transmitting at 4800 bps to have a signal bandwidth greater than 5 kHz. Fig. 8 shows the measured spectrum, which shows a signal bandwidth of about 10 kHz.

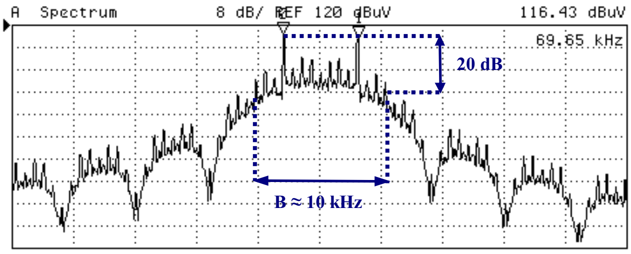


Fig. 8. Measured spectrum of the FSK modulated signal at CISPR 16-1 artificial mains network

The PA output level chosen to achieve compliance with the EN50065-1 document is 128 dBμV rms; this equals to 122 dBμV rms measured at CISPR 16-1 artificial mains network over the whole signal bandwidth, or 116 dBμV rms when measuring the two narrow peaks of the FSK spectrum as in Fig. 8. Setting the output level at 128 dBμV rms, i.e. 7 V peak-to-peak, allows keeping the signal inside the PA output dynamic range, thus ensuring the linearity needed to respect the disturbance mask. This is proven by the measured output spectrum shown in Fig. 9, in which the EN50065-1 conducted disturbance limit mask is drawn for comparison.

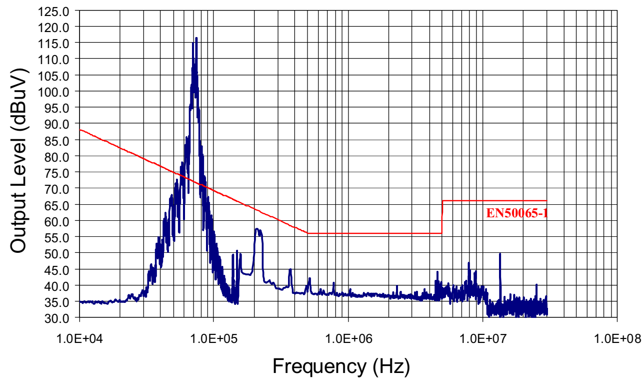


Fig. 9. Output spectrum of the PLC node transmitting at 72 kHz, 4800 baud, deviation 1 measured at CISPR 16-1 artificial mains network, compared with EN50065-1 disturbance limit mask

Once the performance of the circuit in terms of spectral purity has proved to be satisfying, the next check regarded the impedance offered to the line by the PLC node. Results shown in Fig. 10 and Fig. 11 demonstrate the compliance with the EN50065-7 document requirements.

The immunity against the possible interferences from the power line, as listed in the EN50065-2-1 document, has also been tested (see Table I). These tests have made possible to guarantee the capability of the PLC node to operate in a very noisy and disturbing environment like the power line communication scenario.

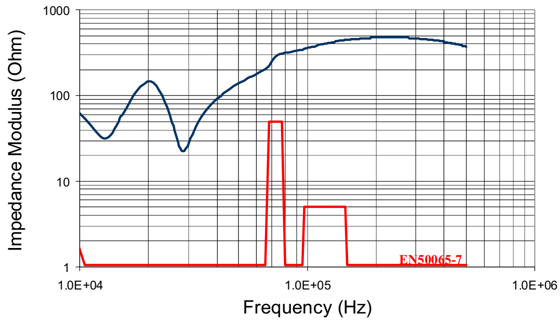


Fig. 10. Input impedance of the PLC node in Reception mode compared with EN50065-7 minimum impedance limit mask

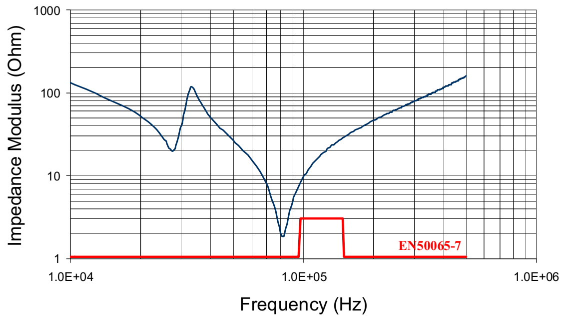


Fig. 11. Input impedance of the PLC node in Transmission mode compared with EN50065-7 minimum impedance limit mask

## V. Thermal Analysis

The power dissipation of the power amplifier stage, driving the power line, is the main cause for the overheating of the PLC transceiver. According to the desired output level ($V_{OUT}$) and the line impedance ($Z_L$), the PA will have to dissipate a power equal to:

$$P_D = \frac{V_{OUT\,rms}^{\;2}}{|Z_L|} \cdot \left( \frac{1}{\eta} - 1 \right). \qquad (1)$$

Assuming $V_{OUT\,rms}$ = 128 dBμV, η = 35% and a typical load impedance of 4Ω, the resulting power to be dissipated would be 2.9 W. Since the ST7540 is hosted in a HTSSOP28 package with exposed pad, exhibiting an asymptotic junction-to-case thermal impedance of 35 °C/W, the junction temperature $T_J$ would reach 131 °C (assuming an ambient temperature $T_A$ = 30 °C) if the transmission was long enough to reach the thermal asymptote. Even though permanent damages to the chip would occur for junction temperature exceeding 170 °C, during normal operating conditions it is however recommended not to surpass 125 °C to ensure a proper functionality of the chip and to avoid affecting its reliability over time.

On the basis of the considerations above, a thermal analysis of the actual behavior of a PLC node is required to guarantee that this condition can be respected.

Since the transmission is typically limited in time, a proper thermal analysis should take into account two aspects:

- the dynamic behavior of the thermal impedance;
- the characteristics of the transmission itself.

### A. Thermal Impedance

The junction temperature $T_J$ can be expressed as follows:

$$T_J(t_{TX}, d) = T_A + P_D \cdot \theta_{JA}(t_{TX}, d), \quad (2)$$

where $\theta_{JA}$ is the junction-to-ambient thermal impedance, which is related to the length of the transmission ($t_{TX}$) and to the duty cycle $d = t_{PKT} / (t_{PKT} + t_{IDLE})$, assuming a packet-fragmented transmission as illustrated by Fig. 12.

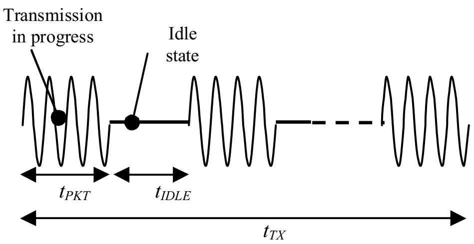


Fig. 12. Packet-fragmented transmission

The thermal impedance $\theta_{JA}$ has been estimated by simulating a 6-cells equivalent model, as shown in Fig. 13. In this model, each cell represents one of the time constants involved in the thermal transient.

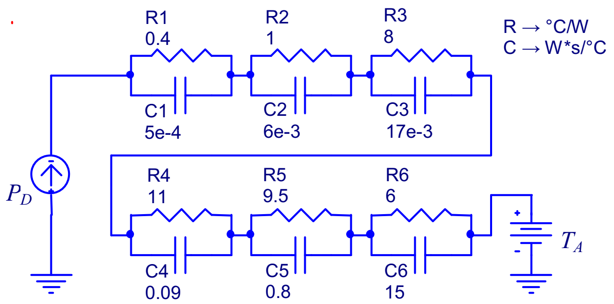


Fig. 13 Equivalent model of the thermal impedance of the HTSSOP28 package with exposed pad

### B. Characteristics of a typical AMR transmission

A typical application of a deployed AMR system is taken into account. AMR networks consist of a master node (concentrator) polling several slave nodes (meters) to collect data about readings. These two classes of nodes (concentrator and meters) are affected by different thermal behavior due to the different operating conditions of the transmission, as described below. The two typical transmission types have been characterized in terms of the resulting thermal impedance and maximum allowed power dissipation.

#### a) Meters

Meters are requested by the concentrator to send data about consumption few times per day. The data are fragmented in 108-bytes packets; taking into account possible repetitions due to bad reception, the traffic amount can be assumed to be 4 packets long in average, with a duty cycle lower than 50%. As the bit rate is 4800 bps, the resulting packet time is $t_{PKT} = 180$ ms and the total transmission time is $t_{TX} = 4^* t_{PKT} / d \approx 1.4$ s.

The above mentioned operating conditions will cause a PLC transceiver in a meter node to get, according to simulation, junction-to-ambient thermal impedance equal to:

$$\theta_{JA}(1.4 \text{ s}, 50\%) = 14 \text{ °C/W}. \quad (3)$$

In order to avoid an overheating of the junction and remain below the safe value of 125 °C in an environment with a $T_A$ = 30 °C, the dissipated power $P_D$ should not exceed:

$$P_D = (125 \text{ °C} - 30 \text{ °C}) / 14 \text{ °C/W} = 6.8 \text{ W}. \quad (4)$$

Experimental measurements have been performed to verify if this limit about power dissipation can be respected. Results are reported at paragraph V.C.

#### b) Concentrator

When polling data from meters, the concentrator usually sends short packets (tens of bytes) to the target node and waits for data. But from time to time the concentrator performs a firmware update requiring the transmission of hundreds of maximum-length packets with a short inter-packet interval, thus leading to high duty cycle. This is the worst-case transmission from the point of view of the thermal transient. We can assume a duty cycle of 90% and transmission duration ($t_{TX}$) of almost 80 s (at 4800 bps).

The PLC transceiver in the concentrator will get, according to simulation, junction-to-ambient thermal impedance equal to:

$$\theta_{JA}(80 \text{ s}, 90\%) = 34 \text{ °C/W}. \quad (5)$$

To keep the device operating in the safe temperature area with ambient temperature $T_A$ = 30 °C, the dissipated power $P_D$ should not exceed:

$$P_D = (125 \text{ °C} - 30 \text{ °C}) / 34 \text{°C/W} = 2.8 \text{ W}. \quad (6)$$

Such dissipating power corresponds, according to Equation 1, to an output level $V_{OUT\,rms}$ = 128 dBμV over a line load $|Z_L|$ = 4.2 Ω. Since the worst-case load at the concentrator should be greater than this value, it can be assumed that power dissipation will not be a limit for the maximum transmitting level of a concentrator node.

Table II summarizes the parameters characterizing the two typical AMR cases.

TABLE II
SUMMARY OF AMR TYPICAL OPERATING CONDITIONS

| Node Type | $t_{TX}$ | $d$ | $\theta_{JA}$ | $P_{D\,max}$ |
|---|---|---|---|---|
| Meter | 1.4 s | 50% | 14 °C/W | 6.8W |
| Concentrator | 80 s | 90% | 34 °C/W | 2.8W |

### C. Experimental Results

Tests have been performed to record the thermal heating of the PLC transceiver in five different conditions of power dissipation. The communication node was configured to emulate the typical traffic of a meter node, i.e. sending a message at 4800 bps, fragmented in four 108 bytes-long packets with a duty cycle of 50%. Five different levels of power dissipation were tested, changing the load impedance ($Z_L$) connected to the power amplifier of the device. For each $Z_L$ value, the voltage output level ($V_{OUT\ rms}$) and power dissipation ($P_D$) were measured and listed in Table III. The case temperature ($T_C$) reached by the device during operation was captured by means of an infrared camera and plotted in

Fig. 14. The maximum value ($T_{C\ max}$) for each condition is reported in Table III.

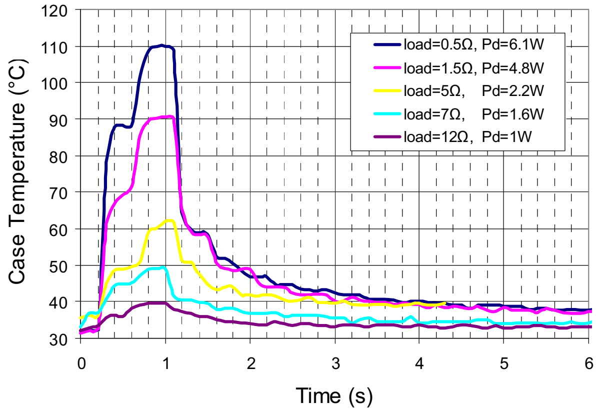


Fig. 14 Transient of the case temperature $T_C$ of the PLC transceiver during transmission with different power dissipation conditions

TABLE III

MEASURED POWER DISSIPATION AND CASE-TO-AMBIENT IMPEDANCE ($\Theta_{CA}$) OF A METER NODE UNDER DIFFERENT IMPEDANCE LOAD CONDITIONS

| $\|Z_L\|$ [Ω] | $V_{OUT\ rms}$ [dBμV] | $T_{C\ max}$ [°C] | $P_D$ [W] | $\theta_{CA}$ [°C/W] |
|---|---|---|---|---|
| 1 Ω | 122 | 110 °C | 6.1 | 14 |
| 1.5 Ω | 126 | 90 °C | 4.8 | 13 |
| 5 Ω | 128 | 60 °C | 2.2 | 14 |
| 7 Ω | 128 | 50 °C | 1.6 | 13 |
| 12 Ω | 128 | 45 °C | 1.0 | 14 |

Table III also shows the equivalent case-to-ambient thermal impedance $\theta_{CA}$ calculated as follows:

$$\theta_{CA} = (T_{C\,max} - 30\ °C) / P_D . \quad (7)$$

The calculated $\theta_{CA}$ can be compared with the expected junction-to-ambient thermal impedance $\theta_{JA}$(1.4s, 50%) = 14 °C/W, as described in previous section. Negligible difference is expected between junction-to-ambient and case-to-ambient thermal impedance. Data listed in Table III, in fact, show a good agreement between simulated $\theta_{JA}$ and measured $\theta_{CA}$ values.

It can be noticed that in the two heaviest load conditions, i.e. $|Z_L|$ = 1.5 Ω and 1 Ω, the PLC transceiver was not able to maintain the output level at 128 dBμV rms because of current limitation. These cases represent extreme line load conditions, possibly related to a short circuit on the line. Nevertheless, even in such extreme conditions, the device showed a good thermal behavior, maintaining the junction temperature below the safe operating limit.

Fig. 15 shows the infrared image captured at the end of the transmission in the case characterized by $|Z_L|$ = 1 Ω and $P_D$ = 6.1 W. The maximum temperature value reached by the PLC transceiver was $T_C$ = 110 °C; the overheating was located on the line driver inside the chip.

As expected, the meter node can dissipate up to about 6 W without undergoing junction overheating.

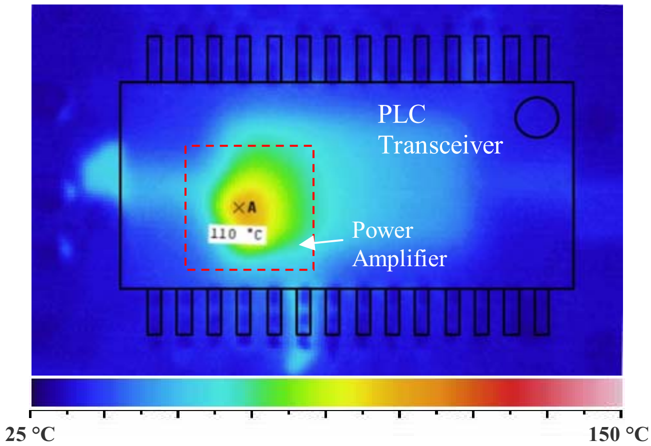


Fig. 15. Infrared photo showing the maximum case temperature ($T_C$ = 110 °C) reached by the PLC transceiver during transmission with $Z_L$ = 1Ω and $P_D$ = 6.1 W. The heating is located on the PA.

## VI. CONCLUSIONS

An in-depth analysis of the electrical requirements for an AMR application has been presented in this paper. These requirements impact mostly on the characteristics of the PLC node that have been described in detail: filtering of the transmitted signal, coupling of the signal to the power line, adequate protection against high energy disturbances, and coexistence between power supply and communication circuitry in terms of noise and impedance. All these aspects have been taken into account in designing the PLC node demonstrator.

On the basis of the considerations reported in this document, it is possible to assert that the adoption of the design criteria described above will allow the development of a low data rate PLC node suitable for AMR applications.

An analysis of the thermal stress of the nodes of an AMR network compliant to Standard EN50065 has been performed. This study has given evidence that a PLC node with the characteristics described in this paper is not subject to critical overheating. In fact, both the typical conditions of the AMR communication and the choice of appropriate thermal impedance for the PLC transceiver allow the device to operate in safe conditions even when transmitting over low impedance offered by the power line.

The same method for evaluating the thermal stress may be applied to any PLC implementation, adapting the considerations presented in this paper to the actual conditions of that particular case.

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